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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,263	05/04/2001	Naoki Furuhashi	PF-2801/NEC/US/mh/B1(ELD)	6317

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EXAMINER

COLEMAN, WILLIAM D

ART UNIT PAPER NUMBER

2823

DATE MAILED: 06/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/848,263

Applicant(s)

FURUHATA, NAOKI

Examiner

W. David Coleman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 May 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-47 and 52 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-47 and 52 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) ✓
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) ✓
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I invention, claims 1-47 and 52 in Paper No. 5 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Prasad et al., U.S. Patent 5,268,315.

4. Prasad discloses a semiconductor device as claimed. See **FIG. 15**, where Prasad teaches a monolithically integrated semiconductor device comprising:

a hetero-junction bipolar transistor having at least an electrode contact layer **86** which contacts directly with at least one of collector, base and emitter electrodes and;

at least a passive device (NiCr Resistor) having at least a passive device electrode **86** (capacitor), and at least a resistive layer,

wherein said electrode contact layer and said resistive layer comprise the same compound semiconductor layer.

Please note, that given the broadest interpretation, silicon nitride is known as a compound semiconductor layer.

5. Pertaining to claim 2, Prasad teaches wherein the said passive device electrode and one of said collector, base and emitter electrodes comprises the same metal layer **86**.
6. Pertaining to claim 3, Prasad teaches wherein said passive device further comprises:
a resistive element (resistor) layer, and at least a resistive element electrode; and
a metal-insulator-metal capacitor (column 7, line 11) which comprises: a bottom electrode; a capacitive dielectric layer; and a top electrode.
7. Pertaining to claim 4, Prasad teaches wherein said at least electrode contact layer comprises a base electrode contact layer which contacts directly with said base electrode.
8. Pertaining to claim 5, Prasad teaches wherein said base electrode contact layer, said resistive element layer and said capacitive dielectric layer comprise the same compound semiconductor layer.
9. Pertaining to claim 6, Prasad teaches wherein said base electrode and said bottom electrode comprise the same metal layer.
10. Pertaining to claim 7, Prasad teaches wherein said base electrode and said top electrode comprise the same metal layer.
11. Pertaining to claim 8, Prasad teaches wherein said base electrode and said resistive element electrodes comprise the same metal layer.
12. Pertaining to claim 9, Prasad teaches wherein said at least electrode contact layer comprises a collector electrode contact layer which contacts directly with said collector electrode.

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13. Pertaining to claim 10, Prasad teaches wherein said collector electrode contact layer, said resistive element layer and said capacitive dielectric layer comprise the same compound semiconductor layer.
14. Pertaining to claim 11, Prasad teaches wherein said collector electrode and said bottom electrode comprise the same metal layer.
15. Pertaining to claim 12, Prasad teaches wherein said collector electrode and said top electrode comprise the same metal layer.
16. Pertaining to claim 13, Prasad teaches wherein collector electrode and said resistive element electrodes comprise the same metal layer.
17. Pertaining to claim 14, Prasad teaches wherein said at least electrode contact layer comprises an emitter electrode contact layer with contacts directly with said emitter electrode.
18. Pertaining to claim 15, Prasad teaches wherein said emitter electrode contact layer, said resistive element layer and said capacitive dielectric layer comprise the same compound semiconductor layer.
19. Pertaining to claim 16, Prasad teaches wherein said emitter electrode and said bottom electrode comprise the same metal layer.
20. Pertaining to claim 17, Prasad teaches wherein said emitter electrode and said top electrode comprise the same metal layer.
21. Pertaining to claim 18, Prasad teaches wherein said emitter electrode and said resistive element electrodes comprise the same metal layer.
22. Pertaining to claim 19, Prasad teaches wherein said at least passive device further comprises:

a resistive element which comprises: at least a resistive element layer; and at least a resistive element electrode.

23. Pertaining to claim 20, Prasad teaches wherein said at least electrode contact layer comprises a base electrode contact layer which contacts directly with said base electrode.

24. Pertaining to claim 21, Prasad teaches wherein said base electrode contact layer and said resistive element layer comprise the same compound semiconductor layer.

25. Pertaining to claim 22, Prasad teaches wherein said base electrode and said resistive element electrodes comprise the same metal layer.

26. Pertaining to claim 23, Prasad teaches wherein said at least electrode contact layer comprises a collector electrode contact layer which contacts directly with said collector electrode.

27. Pertaining to claim 24, Prasad teaches wherein said collector electrode contact layer and said resistive element layer comprise the same compound semiconductor layer.

28. Pertaining to claim 25, Prasad teaches wherein said collector electrode and said resistive element electrodes comprise the same metal layer.

29. Pertaining to claim 26, Prasad teaches wherein said at least electrode contact layer comprises an emitter electrode contact layer which contacts directly with said emitter electrode.

30. Pertaining to claim 27, Prasad teaches wherein said emitter electrode contact layer and said resistive element layer comprise the same compound semiconductor layer.

31. Pertaining to claim 28, Prasad teaches wherein said emitter electrode and said resistive element electrodes comprise the same metal layer.

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32. Pertaining to claim 29, Prasad teaches wherein said at least passive device further comprises:

a metal-insulator-metal capacitor which comprises: a bottom electrode; a capacitive dielectric layer; and a top electrode.

33. Pertaining to claim 30, Prasad teaches wherein said at least electrode contact layer comprises a base electrode contact layer which contacts directly with said base electrode.

34. Pertaining to claim 31, Prasad teaches wherein said base electrode contact layer and said capacitive dielectric layer comprise the same compound semiconductor layer.

35. Pertaining to claim 32, Prasad teaches wherein said base electrode and said bottom electrode comprise the same metal layer.

36. Pertaining to claim 33, Prasad teaches wherein said base electrode and said top electrode comprise the same metal layer.

37. Pertaining to claim 34, Prasad teaches wherein said at least electrode contact layer comprises a collector electrode contact layer which contacts directly with said collector electrode.

38. Pertaining to claim 35, Prasad teaches wherein said collector electrode contact layer and said capacitive dielectric layer comprise the same compound semiconductor layer.

39. Pertaining to claim 36, Prasad teaches wherein said collector electrode and said bottom electrode comprise the same metal layer.

40. Pertaining to claim 37, Prasad teaches wherein said collector electrode and said top electrode comprise the same metal layer.

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41. Pertaining to claim 38, Prasad teaches wherein said at least electrode contact layer comprises an emitter electrode contact layer which contacts directly with said emitter electrode.

42. Pertaining to claim 39, Prasad teaches wherein said emitter electrode contact layer and said capacitive dielectric layer comprise the same compound semiconductor layer.

43. Pertaining to claim 40, Prasad teaches wherein said emitter electrode and said bottom electrode comprise the same metal layer.

44. Pertaining to claim 41, Prasad teaches wherein said emitter electrode and said top electrode comprise the same metal layer.

45. Pertaining to claim 42, Prasad teaches a monolithically integrated semiconductor device comprising:

a hetero-junction bipolar transistor having at least an electrode contact layer which contacts directly with at least one of collector, base and emitter electrodes; and

at least a passive device having at least a passive device electrode and at least a resistive layer,

wherein said passive device electrode and one of said collector, base and emitter electrodes comprises the same metal layer.

46. Pertaining to claim 43, Prasad teaches wherein said electrode contact layer and said resistive layer comprise the same compound semiconductor layer.

47. Pertaining to claim 44, Prasad teaches wherein said at least passive device further comprises:

a resistive element which comprises: at least a resistive element layer; and at least a resistive element electrode; and

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a metal-insulator-metal capacitor which comprises: a bottom electrode; a capacitive dielectric layer; and a top electrode.

48. Pertaining to claim 45, Prasad teaches wherein said at least passive device further comprises:

a resistive element which comprises: at least a resistive element layer; and at least a resistive element electrode.

49. Pertaining to claim 46, Prasad teaches wherein said at least passive device further comprises : a bottom electrode; a capacitive dielectric layer; and a top electrode.

50. Pertaining to claim 47, Prasad teaches a monolithically integrated semiconductor device comprising:

a hetero-junction bipolar transistor having at least an electrode contact layer which contacts directly with at least one of collector, base and emitter electrodes;

a resistive element which comprises: at least a resistive element layer; and at least a resistive element electrode; and

a metal-insulator-metal capacitor which comprises a bottom electrode; a capacitive dielectric layer; and a top electrode,

wherein said electrode contact layer, said resistive element layer and said capacitive dielectric layer comprise the same compound semiconductor layer, and

wherein said resistive element electrode, said top electrode and said at least one of collector, base and emitter electrodes comprises the same metal layer.

51. Pertaining to claim 52, Prasad teaches a monolithically integrated semiconductor device comprising: a hetero-junction bipolar transistor having at least an electrode contact layer which

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contacts directly with at least one of collector, base and emitter electrodes; a resistive element which comprises : at least a resistive element layer; and at least a resistive element electrode; and a metal-insulator-metal capacitor which comprises : a bottom electrode; a capacitive dielectric layer; and a top electrode,

wherein said electrode contact layer, said resistive element layer and said capacitive dielectric layer are formed concurrently in the same processes, and

wherein said resistive element electrode, said top electrode and said at least one of collector, base and emitter electrodes are formed concurrently in the same processes.

52. Pertaining to claim 52, even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

53. “The Patent Office bears a lesser burden of proof in making out a case of *prima facie* obviousness for product-by-process claims because of their peculiar nature: than when a product is claimed by conventional fashion. *In re Fessmann*, 489 F.2d 742, 744, 180 USPQ 324, 326 (CCPA 1974). Once the Examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to Applicant to come forward with evidence establishing an unobvious

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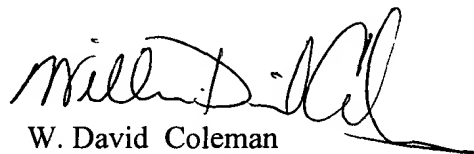
difference between the claimed product and the prior art product. *In re Marosi*, 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983).

Conclusion

54. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



W. David Coleman
Examiner
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WDC
June 12, 2002